register rather than two flip-flops, the load on the clock can be reduced, thereby achieving reduced propagation delay. To further improve the performance of the finite impulse response filter, a simpler carry-save adder is employed in the least significant bit section, which is possible due to the use of a single register at an input to each of the carry-save adders rather than two flip-flops, one for a carry output and one for a sum output from the adder. The combination of a reduction of half of the flip-flops and a replacement of a simpler carry-save adder for each of the carry-save adders results in a significant improvement in the overall filter performance and power and space consumption.

REMARKS

Amendment to the Specification

Applicants amended the Specification to add the cross-reference information with the parent case and to correct a typographical error. Examiner is requested to review and enter the change. No new matter is added as a result of these changes.

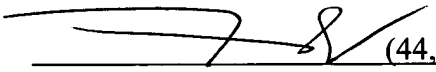
Amendment to the Abstract

Applicants amended the Abstract as suggested by the Examiner in an office action in the parent case. No new matter is added as a result of this change.

Conclusion

This is a preliminary amendment filed with the divisional application. No fee is due with this response.

Respectfully Submitted,



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ABSTRACT

A partial carry-save format is employed for a finite impulse response filter output representation, thereby reducing a number of flip-flops and hence power. By replacing the least significant bit processing section on the output side of the finite impulse response filter with a combined carry-save adder and carry-propagate adder followed by a register rather than two flip-flops, the load on the clock can be reduced, thereby achieving reduced propagation delay. To further improve the performance of the finite impulse response filter, a simpler carry-save adder is employed in the least significant bit section, which is possible due to the use of a single register at an input to each of the carry-save adders rather than two flip-flops, one for a carry output and one for a sum output from the adder. The combination of a reduction of half of the flip-flops and a replacement of a simpler carry-save adder for each of the carry-save adders results in a significant improvement in the overall filter performance and power and space consumption.